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NOTICE OF ALLOWANCE AND FEE(S) DUE

59796 7590 10/16/2009

INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
UNELUS, ERNEST	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/16/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,872	04/20/2004	Kenneth C. Creta	P18867	5618

TITLE OF INVENTION: WRITE COMBINING PROTOCOL BETWEEN PROCESSORS AND CHIPSETS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	01/19/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

59796 7590 10/16/2009

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,872	04/20/2004	Kenneth C. Creta	P18867	5618

TITLE OF INVENTION: WRITE COMBINING PROTOCOL BETWEEN PROCESSORS AND CHIPSETS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	01/19/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
UNELUS, ERNEST	2181	710-005000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

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❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNELUS, ERNEST	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/16/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 215 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 215 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/828,872	CRETA ET AL.	
	Examiner	Art Unit	
	ERNEST UNELUS	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/07/09*.

2. ☒ The allowed claim(s) is/are *1-19,21-29 and 34-36*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

I. EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. David P. McAbee (Reg. No. 58,104) on October 7, 2009. The examiner proposed amendments to better place the application in condition for allowance, particularly adding the limitation that prior arts fail to teach. Mr. McAbee agreed.

The application has been amended as follows:

3. **Claim 1** (Currently Amended) A method comprising:

receiving a plurality of write transactions with a controller hub from a processor ~~requesting device~~, each of the plurality of write transactions being associated with a write combinable attribute to indicate they are a plurality of write combinable write transactions;

buffering data associated with the plurality of write combinable write transactions in a buffer of the controller hub in response to each of the plurality of write transactions being associated with the write combinable attribute to indicate they are the write combinable write transactions; and

transmitting a write completion signal corresponding to each of the plurality of write combinable write transactions with the controller hub to the processor ~~requesting device~~ in

response to buffering the data associated with each of the plurality of write combinable write transactions;

flushing the data associated with the plurality of write combinable write transactions in the buffer as write combined data in a single transaction to an I/O device in response to receiving a flush signal from the processor ~~requesting device~~ after transmitting the write completion signal corresponding to each of the plurality of write combinable write transactions with the controller hub to the processor.

4. **Claim 2** (Currently Amended) The method of claim 1, wherein the processor ~~requesting device~~ is to transmit the flush signal in response to receiving a last write completion corresponding to a last write combinable write transaction of the plurality of write combinable write transactions.

5. **Claim 3** (Currently Amended) The method of claim 2, wherein the write completion signal corresponding to each of the plurality of write transactions is transmitted by the controller hub before the processor ~~requesting device~~ transmits the flush signal, and wherein the controller hub is further to transmit a flush completion signal to the processor ~~requesting device~~ in response to flushing the data to the I/O device.

6. **Claim 4** (Currently Amended) The method of claim 3, wherein the processor ~~requesting device~~ is not to issue any further write combinable writes to a same memory region associated with the plurality of write combinable write transactions from when the flush signal is

transmitted by the processor ~~requesting device~~ to when the processor ~~requesting device~~ receives the flush completion signal.

7. **Claim 5** (Currently Amended) The method of claim 1, wherein flushing the data as write combined data to the I/O device in response to receiving the flush signal from the processor ~~requesting device~~ further includes: tagging the buffer with a first source identifier associated with one or more of the write combinable write transactions and the processor ~~requesting device~~; detecting a second source identifier associated with the flushing signal; comparing the second source identifier to the first source identifier; and flushing the data as write combined data to the I/O device in response to the second source identifier matching the first source identifier.

8. **Claim 6** (Original) The method of claim 5, further including repeating the comparing for a plurality of buffers, each buffer corresponding to an I/O port.

9. **Claims 7-9** (Canceled).

10. **Claim 10** (Currently Amended) The method of claim 1, wherein the write combined data includes more than one cache line worth of data.

11. **Claim 11** (Original) The method of claim 1, wherein the receiving includes receiving a plurality of commands instructing the hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

12. **Claim 12** (Currently Amended) An apparatus comprising: a hub to be coupled to a processor, the hub including:

receiving logic to receive a first write transaction and a second write transaction from a processor, the first and the second write transactions to reference partial data of a cache line within the processor, wherein the first and second write transactions include a write combinable attribute to indicate a first and a second partial write transactions as write combinable,

combining logic coupled to the receiving logic to combine the partial data of the cache line referenced by the first and second write transactions as write combined data in response to the first and second write transactions including the write combinable attribute to indicate they are write combinable; and

flushing logic coupled to the combining logic to flush the write combined data in a single transaction to an I/O device in response to a flush protocol event.

13. **Claim 13** (Previously Amended) The apparatus of claim 12, wherein the flush protocol event includes special flush signal to be received by the receiving logic from the processor.

14. **Claim 14** (Previously Amended) The apparatus of claim 13, further comprising transmission logic to send a first and a second write completion signals to the processor for the first and the second write transactions, respectively, before the write combined data is flushed to the I/O device, wherein the first and the second write completion signals are to verify successful storage of the partial data referenced by the first and the second write transactions, respectively.

15. **Claim 15** (Previously Amended) The apparatus of claim 14, wherein the transmission logic is also to send a flush completion signal to the processor after the write combined data is flushed to the I/O device.

16. **Claim 16** (Previously Amended) The apparatus of claim 12, further comprising latency logic coupled to the combining logic to detect occurrence of a latency condition, wherein the flush protocol event includes occurrence of the latency condition.

17. **Claim 17** (Previously Amended) The apparatus of claim 16, further comprising transmission logic to send a first and a second write completion signals to the processor for the first and the second write transactions, respectively, as the write combined data is flushed to the I/O device, wherein the first and the second write completion signals are to verify flushing of the first and the second write transactions, respectively.

18. **Claim 18** (Previously Amended) The apparatus of claim 16, wherein the latency condition includes a delay in receiving a next third combinable write transaction from the processor and an interface to the I/O device being in an idle state.

19. **Claim 19** (Previously Amended) The apparatus of claim 12, wherein the combining logic includes a plurality of buffers, each buffer corresponding to an I/O port, and wherein the flushing

logic is to flush data from one of the plurality of buffers corresponding to the processor in response to a flush protocol event associated with the processor.

20. **Claim 20** (Cancelled).

21. **Claim 21** (Currently Amended) An apparatus comprising:

a hub to be coupled to a first device and a second device, the hub including:

a buffer;

receiving logic to receive a first combinable write transaction and a second combinable write transaction from the first device; and

a write combining module to

store first data associated with the first combinable write transaction in the buffer and send a first write completion signal to the first device in response to storing the first data in the buffer,

store second data associated with the second combinable write transaction in the buffer and send a second write completion signal to the first device in response to storing the second data in the buffer, and

flush the first data and the second data as combined data in a single transaction to the second device in response to receiving a flush signal from the first device.

22. **Claim 22** (Currently Amended) The apparatus of claim 21, wherein the first device includes a processor and the second device include an input/output (I/O) device.

23. **Claim 23** (Previously Amended) The apparatus of claim 22, wherein the processor is to generate the flush signal in response to a flushing event, the flushing event being selected from a group consisting of use of an ordering fence, encountering an implicit locked instruction, and encountering an interrupt.

24. **Claim 24** (Previously Amended) The apparatus of claim 23, wherein the processor is to generate the flush signal further in response to a write combine history indicating the first combinable write transaction and the second write combinable transaction have been issued by the processor.

25. **Claim 25** (Previously Amended) The apparatus of claim 22, wherein the write combining module is further to send a flush completion signal to the processor in response to the flush of the first data and the second data as combined data to the I/O device.

26. **Claim 26** (Previously Amended) The apparatus of claim 25, wherein the processor is not to issue any further write combinable write transactions to a memory region associated with the first and the second combinable write transactions from when the processor generates the flush signal to when the processor receives the flush completion signal.

27. **Claim 27** (Previously Amended) The apparatus of claim 22, wherein the write combining module is to be implemented in a layered communication protocol including at least a physical layer and a link layer.

28. **Claim 28** (Previously Amended) The apparatus of claim 27, wherein the hub is to be coupled to the processor though a point-to-point interconnect.

29. **Claim 29** (Previously Amended) The apparatus of claim 21, wherein the write combining module is further to flush the first data and the second data as combined data to the second device in response to receiving the flush signal from the first device comprises: determine the flush signal is from the first device based on a first source identifier associated with the first and second combinable write transactions matching a second source identifier associated with the flush signal.

30. **Claims 30-33** (Cancelled).

31. **Claim 34** (Currently Amended) An apparatus comprising:

a processor including:

write logic to transmit a plurality of write transactions to be identified as write combinable to a hub;

receiving logic to receive a write completion for each of the plurality of write transactions from the hub;

protocol logic to transmit a flush signal to the hub to initiate a flush of data associated with the plurality of write transactions in a single transaction to an I/O device in response to detecting a flush event and in response to receiving, with the receiving logic, a last write completion for a last write transaction of the plurality of write transactions.

32. **Claim 35** (Previously Amended) The apparatus of claim 34, wherein the flush event is selected from a group consisting of use of an ordering fence, encountering an implicit locked instruction, and encountering an interrupt.

33. **Claim 36** (Previously Amended) The apparatus of claim 34, wherein the protocol logic is further to not allow the write logic to transmit any further write transactions to be identified as write combinable to a memory region associated with the plurality of write transactions from when the protocol logic transmits the flush signal to when the receiving logic receives a flush completion signal from the hub to indicate the flush of the data associated with the plurality of write transactions has been performed.

34. **Claims 37-39** (Cancelled).

II. RELEVANT ART CITED BY THE EXAMINER

1. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

2. The following reference teaches write transactions on an input/output (I/O) hub according to a protocol between the target and a processor.

U.S. PATENT NUMBER

US 6,950,438; 6,457,084; 6,877,049; 6,601,118; 2003/0023666; 2005/0071534; 2004/0015503; 6,101,568; 2002/0087801

III. ALLOWABLE SUBJECT MATTER

1. The following is an examiner's statement of reasons for allowance: In regards to claims 1, 12, 21, and 34, the closest prior arts fail to disclose "flushing the data associated with the plurality of write combinable write transactions in the buffer as write combined data in a single transaction to an I/O device in response to receiving a flush signal from the processor after transmitting the write completion signal corresponding to each of the plurality of write combinable write transactions with the controller hub to the processor".

2. The remaining claims 2-11, 13-19, 22-29, and 35-36 are allowed by virtue of their dependencies on the independent claims. Hence, the examiner has allowed claims 1-19, 21-29, and 34-36.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

IV. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

1. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS ALOWED IN THE APPLICATION

2. Per the instant office action, claims 1-19, 21-29, and 34-36 have been allowed.

b. DIRECTION OF FUTURE CORRESPONDENCES

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

4. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181
October 7, 2009

Ernest Unelus
Patent Examiner
Art Unit 2181

/Ernest Unelus/
Examiner, Art Unit 2181